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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,704	12/06/2001	Sang-Ho Ahn	9903-045	8392

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MARGER JOHNSON & McCOLLOM, P.C.
1030 S.W. Morrison Street
Portland, OR 97205

EXAMINER	
TRAN, TAN N	

ART UNIT	PAPER NUMBER
2826	7

DATE MAILED: 09/23/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/008,704	AHN ET AL.	
	Examiner	Art Unit	
	TAN N TRAN	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29 and 50-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19,23-29 and 50-53* is/are rejected.

7)☒ Claim(s) *20-22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restriction

1. Applicant's election without traverse of Group I, claims 1-29,50-53 in Paper No. 6 is acknowledged.

Oath/Declaration

2. The oath/declaration filed on 12/06/01 is acceptable.

Information Disclosure Statement

3. If applicant is aware of any relevant prior art, he/she requested to cite it on form PTO-1449 in accordance with the guidelines set forth in M.P.E.P. 609.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 8,19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 8, lines 1-3, what does applicant mean by "upper and lower portions of the package body with reference to the leads have different thickness each other"?

In claim 19, lines 1-3, what does applicant mean by "the package body has an upper thickness difference from a lower thickness thereof, when view with reference to the leads."?

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3,5,8-10,50 are rejected under 35 U.S.C. 102(b) as being anticipated by Casto et al. (5,014,113).

With regard to claims 1,50 Casto et al. discloses a lead frame comprising a die pad 40, a plurality of leads (18,28) disposed around the die pad 40 and a tie bars 46 connected to and disposed around the die pad 40, wherein the die pad 40 comprises a chip attaching part and a peripheral part surrounding the chip attaching part; a semiconductor chip 12 mounted to the die pad chip attaching part, the chip 12 having a plurality of electrode pads 14, wherein the plurality of electrode pads 14 are electrically interconnected to the leads (18,28), and wherein each of leads (18,28) comprises integrally connected inner leads and outer leads; an encapsulant encapsulating the semiconductor chip 12 to form a package body 36, wherein the inner leads are encapsulated by the encapsulant and the outer leads are external to the encapsulant; and the chip

attaching part having a first thickness and the inner leads (portion of leads 18 and 28) having a second thickness greater than the first thickness. (Note figs.1, 2 of Casto et al.).

With regard to claim 2, Casto et al. discloses the first thickness is between about 30 percent to 50 percent of the second thickness. (Note fig.1 of Casto et al.).

With regard to claim 3, Casto et al. discloses the chip attaching part and the peripheral part have the same thickness. (Note fig.1 of Casto et al.).

With regard to claim 5, Casto et al. discloses the die pad 40 is located below the leads 28. (Note fig.1 of Casto et al.).

With regard to claim 8, Casto et al. discloses upper and lower portions of the package body with reference to the leads (18,28) have different thickness each other. (Note fig.1 of Casto et al.).

With regard to claim 9, Casto et al. discloses the tie bar 46 has the same thickness as the leads 18. (Note figs.1,2 of Casto et al.).

With regard to claim 10, Casto et al. discloses the tie bar 46 has the same thickness as the die pad peripheral part. (Note figs.1,2 of Casto et al.).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4,6,7,12-14,51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Casto et al. (5,014,113) in view of Huang (2002/0113305).

With regard to claim 4, Casto et al. does not disclose two semiconductor chips each attached to a corresponding side of the die pad chip attaching part.

However, Huang discloses two semiconductor chips (12a,12b) each attached to a corresponding side of the die pad chip attaching part. (Note Fig. 6 of Huang).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Casto et al.'s device having two semiconductor chips each attached to a corresponding side of the die pad chip attaching part such as taught by Huang in order to obtain a compact package of integrated circuit.

With regard to claim 6, Casto et al. discloses the plurality of electrode pads 14 are electrically interconnected to the leads (18,28) via bonding wires 34.

Casto et al. and Huang do not disclose bonding wires are connected by balls formed on the surface of the leads and stiches formed on the electrode pads. However, it would have been obvious to one of ordinary skill in the art to form bonding wires are connected by balls formed on the surface of the leads and stiches formed on the electrode pads in order to secure the interface between semiconductor chips and the die pads.

With regard to claim 7, Casto et al. discloses metal bumps are formed on the electrode pads 14 of the chip 12. (Note lines 1-7, column 4, fig. 1 of Casto et al.).

Casto et al. and Huang do not disclose the stiches are formed on the metal bumps. However, it would have been obvious to one of ordinary skill in the art to form the stiches are formed on

the metal bumps in order to secure the interface between semiconductor chips and the die pads. (Note lines 1-7, column 4, fig. 1 of Casto et al.).

With regard to claim 12, Huang discloses the die pad comprises divided first and second die pads (410,440). (Note fig. 1 of Huang).

With regard to claim 13, Huang discloses the first and second die pads (410,440) each include a chip attaching part and a peripheral part. (Note fig. 1 of Huang).

With regard to claim 14, Huang discloses an adhesive 11a bonds the semiconductor chip to the die pad chip attaching part. (Note fig. 6 of Huang).

With regard to claim 51, Huang and Casto et al. disclose all the claimed subject matter except for the electronic apparatus is a memory card. However, it would have been obvious to one of ordinary skill in the art to form the electronic apparatus is a memory card, because such structure is conventional in the art for forming a compact multi-chip package.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Casto et al. (5,014,113) in view of Kouda (5,818,105).

Casto et al. does not disclose the peripheral part protrudes in both vertical directions from the chip attaching part, and the thickness of the peripheral part is equal to the thickness of the leads.

However, Kouda discloses the peripheral part protrudes in both vertical directions from the chip attaching part, and the thickness of the peripheral part is equal to the thickness of the leads 83. (Note fig. 8 of Kouda).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Casto et al.'s device having the peripheral part protrudes in both vertical directions from the chip

attaching part, and the thickness of the peripheral part is equal to the thickness of the leads such as taught by Kouda in order to secure the semiconductor chip on the die pad of the lead frame.

Claims 15,16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Casto et al. (5,014,113) in view of Huang (2002/0113305) and further in view of Kozono (6,177,718).

With regard to claim 15, Casto et al. and Huang does not disclose the lead frame is made of iron-nickel alloy or copper alloy, and wherein the bonding wires are gold wires.

However, Kozono discloses the lead frame 13 is made of iron-nickel alloy or copper alloy, and wherein the bonding wires 14 are gold wires. (Note lines 16-20, column 6, fig. 21 of Kozono).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Casto et al. and Huang's device having the lead frame is made of iron-nickel alloy or copper alloy, and wherein the bonding wires are gold wires such as taught by Kozono in order to prevent the lead frame from broken.

With regard to claim 16, Kozono, Casto et al. and Huang do not disclose the semiconductor chip is a memory device and wherein the adhesive is a film made of an epoxy resin. However, it would have been obvious to one of ordinary skill in the art to form the semiconductor chip is a memory device and wherein the adhesive is a film made of an epoxy resin in order to secure the semiconductor chip on the die pad of the lead frame and because such structure is conventional in the art for forming a compact multi-chip package.

Claims 17-19,23-29,52,53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kouda (5,818,105) in view of Huang (2002/0113305).

With regard to claims 17, 52, Kouda discloses a lead frame having a die pad 89a, a plurality of leads 83 disposed around the die pad 89a, the die pad 89a including attaching part having a first thickness and a peripheral part surrounding and protruding away from the chip attaching part; the leads 83 having inner leads encapsulated with the package body to which the bonding wires 86 and bonded and outer leads exposed from the package body, wherein the inner leads having a second thickness, wherein the first thickness is smaller than the second thickness, and wherein the peripheral part has a thickness equal to the second thickness of the inner leads. (Note Fig. 8 of Kouda).

Kouda does not disclose a tie bar connected to the die pad, and first and second semiconductor chips each having a plurality of electrode pads formed on an active surface of the chip, the first chip being attached to a top surface of the chip attaching part and the second chip being attached to a bottom surface of the chip attaching part.

However, Huang discloses a tie bar connected to the die pad 10, and first and second semiconductor chips (12a,12b) each having a plurality of electrode pads formed on an active surface of the chip, the first chip being attached to a top surface of the chip attaching part and the second chip being attached to a bottom surface of the chip attaching part. (Note lines 1-6, paragraph 0047, page 4, figs. 2,6 of Huang).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Kouda's device having a tie bar connected to the die pad, and first and second semiconductor chips each having a plurality of electrode pads formed on an active surface of the chip, the first

chip being attached to a top surface of the chip attaching part and the second chip being attached to a bottom surface of the chip attaching part such as taught by Huang because such structure is conventional in the art for forming a lead frame.

With regard to claim 18, Kouda discloses the die pad 89a peripheral part protrudes toward the semiconductor chip 84. (Note fig. 8 of Kouda).

With regard to claim 19, Kouda discloses upper and lower portions of the package body with reference to the leads 83 have different thickness each other. (Note fig. 8 of Kouda).

With regard to claim 23, Kouda and Huang do not disclose bonding wires are connected by balls formed on the surface of the leads and stiches formed on the electrode pads. However, it would have been obvious to one of ordinary skill in the art to form bonding wires are connected by balls formed on the surface of the leads and stiches formed on the electrode pads in order to secure the interface between semiconductor chips and the die pads.

With regard to claim 24, Kouda and Huang do not disclose metal bumps are formed on the electrode pads of the chip and wherein the stiches are formed on the metal bumps. However, it would have been obvious to one of ordinary skill in the art to form metal bumps are formed on the electrode pads of the chip and wherein the stiches are formed on the metal bumps in order to secure the interface between semiconductor chips and the die pads.

With regard to claim 25, Huang discloses the die pad comprises divided first and second die pads (410,440). (Note fig. 1 of Huang).

With regard to claim 26, Huang discloses the first and second die pads (410,440) each include a chip attaching part and a peripheral part. (Note fig. 1 of Huang).

With regard to claim 27, Huang discloses an adhesive 11a bonds the semiconductor chip to the die pad chip attaching part. (Note fig. 6 of Huang).

With regard to claim 28, Kouda and Huang disclose all the claimed subject matter except for a thickness of the package body is about 580 micrometer, a thickness of the die pad peripheral part is about 100 micrometer, and a thickness of the chip attaching part is about 40 micrometer. However, it would have been obvious to one of ordinary skill in the art to form for a thickness of the package body is about 580 micrometer, a thickness of the die pad peripheral part is about 100 micrometer, and a thickness of the chip attaching part is about 40 micrometer in order to simplify the structure and fabrication to reduce the assembly cost of the device and to reduce the thickness or height of the device, because such structure is conventional in the art for forming a compact multi-chip package.

With regard to claim 29, Huang discloses an adhesive is attached to the backside of the chip in a wafer state to bond the semiconductor chips (12a,12b) to the chip attaching part. (Note fig. 6 of Huang).

With regard to claim 53, Kouda, and Huang disclose all the claimed subject matter except for the electronic apparatus is a memory card. However, it would have been obvious to one of ordinary skill in the art to form the electronic apparatus is a memory card, because such structure is conventional in the art for forming a compact multi-chip package.

Allowable Subject Matter

7. Claims 20-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 20-22 are allowable over the prior art of record, because none of these references disclose or can be combined to yield the claimed invention such as the peripheral part protrudes toward the second semiconductor chip as recited in claim 20, and the bonding wires connected to one of the semiconductor chips are shorter than the bonding wires connected to the other semiconductor chip as recited in claim 22.

Conclusion

8. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Tan Tran whose telephone number is (703) 305-3362. The examiner can normally be reached on M-F 8:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for after final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

TT

April 2002

Minh Loan Tran
Primary Examiner